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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,620	07/01/2004	Jigang Liu	CN 020002	4330

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EXAMINER	
NGUYEN, TUAN HOANG	
ART UNIT	**PAPER NUMBER**
2618	

NOTIFICATION DATE	DELIVERY MODE
09/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/500,620	LIU, JIGANG	
	Examiner	Art Unit	
	Tuan H. Nguyen	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-6 and 8-20* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/06/2007 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5-6, and 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US PAT. 5,319,798) in view Na (US PAT. 6,226,276).

Consider claim 1, Watanabe teaches a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a single digital synthesizer driven phase locked loop, wherein said digital synthesizer driven phase locked loop, in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop, in said receiving mode, being in an oscillating state and receiving a non-modulation signal (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that digital synthesizer driven phase locked loop comprises, in said modulating stale, a first filtering performance, with said digital synthesizer driven phase locked loop comprising, in said oscillating state, a second filtering performance different from said first filtering performance.

In the same field of endeavor, Na teaches digital synthesizer driven phase locked loop comprises, in said modulating stale, a first filtering performance, with said digital synthesizer driven phase locked loop comprising, in said oscillating state, a second filtering performance different from said first filtering performance (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, digital synthesizer driven phase locked loop comprises, in said modulating stale, a first filtering performance, with said digital synthesizer driven phase locked loop comprising, in said oscillating state, a second filtering performance different from said first filtering performance, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio

communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

Consider claim 3, Na further teaches characterized in that transceiver comprises a controller for generating modulation signal and for generating control signals, with a switch being coupled to controller and digital synthesizer driven phase locked loop for in response to a first control signal supplying modulation signal from controller to digital synthesizer driven phase locked loop and in response to a second control signal supplying non-modulation signal to digital synthesizer driven phase locked loop (col. 7 line 39 through col. 8 line 29).

Consider claim 5, Watanabe teaches 5. (Currently amended) A transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a single digital synthesizer driven phase locked loop, wherein said digital synthesizer driven phase locked loop, in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop, in said receiving mode, being in an oscillating state (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to

said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter.

In the same field of endeavor, Na teaches single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

Consider claim 6, Na further teaches characterized in that digital synthesizer driven phase locked loop, in modulating state, generates a modulated signal, with digital synthesizer driven phase locked loop, in oscillating state, generating a non-modulated signal (col. 7 line 39 through col. 8 line 29).

Consider claim 8, Watanabe teaches a single digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said single digital Synthesizer driven phase locked loop, wherein said single digital synthesizer driven phase locked loop, in said transmitting mode, is in a modulating state, with said single digital synthesizer driven phase locked loop, in said receiving mode, being in an oscillating state (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said fast filter and in response to a second control signal selecting said second filter.

In the same field of endeavor, Na teaches digital single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said fast filter and in response to a second control signal selecting said second filter (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said fast filter and in response to a second control signal selecting said second filter, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio

communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

Consider claim 9, Watanabe teaches a phase locked loop for use in a single digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said digital synthesizer driven phase locked loop, wherein said phase locked loop, in said transmitting mode, is in a modulating state, with said phase locked loop, in said receiving mode, being in an oscillating state (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter.

In the same field of endeavor, Na teaches single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, single digital synthesizer driven phase locked loop

comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

Consider claim 10, Watanabe teaches a digital synthesizer for use in a single digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said digital synthesizer &iven phase locked loop, wherein said digital synthesizer, in said transmitting mode, is in a modulating state, with said digital synthesizer, in said receiving mode, being in an oscillating state (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second Falter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter.

In the same field of endeavor, Na teaches single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second Falter for in response to a first control signal selecting

said first filter and in response to a second control signal selecting said second filter (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second Falter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

Consider claim 11, Watanabe teaches a system comprising at least one portable unit and at least one network trait for radio communication, with at least one unit comprising at least one transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a single digital synthesizer driven phase locked loop, wherein said digital synthesizer driven phase locked loop, in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop, in said receiving mode, being in an oscillating state (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to

said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter.

In the same field of endeavor, Na teaches single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

Consider claim 12, Watanabe teaches a portable unit comprising a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a single digital synthesizer driven phase locked loop, wherein said digital synthesizer driven phase locked loop, in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop, in said

receiving mode, being in an oscillating state (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter.

In the same field of endeavor, Na teaches single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

Consider claim 13, Watanabe teaches a network trait comprising at least one transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a single digital *synthesizer* driven phase locked loop, wherein said digital synthesizer drive phase locked loop, in said transmitting mode, is in a modulating state, with said digital synthesizer drive phase locked loop, in said receiving mode, being in an oscillating state (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter.

In the same field of endeavor, Na teaches single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio

communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

Consider claim 14, Watanabe teaches a method for transmitting signals in a transmitting mode and for receiving signals in a receiving mode via a single digital synthesizer driven phase locked loop, wherein said method comprises the acts of: bringing said digital synthesizer driven phase locked loop, in said transmitting mode, in a modulating state, and et in said receiving mode, bringing said digital synthesizer driven phase locked loop in an oscillating state (figs. 1 and 3 col. 1 lines 58-67 and col. 5 lines 37-59).

Watanabe does not explicitly show that single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter.

In the same field of endeavor, Na teaches single digital synthesizer driven phase locked loop comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter (figs. 1 and 3, col. 7 line 39 through col. 8 line 29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, single digital synthesizer driven phase locked loop

comprises a first filter and a second filter, with a switch being coupled to said first filter and said second filter for in response to a first control signal selecting said first filter and in response to a second control signal selecting said second filter, as taught by Na, in order to provide a circuit and process for operating a time division duplex digital radio communication system able to quickly stabilize the transmission intermediate frequency during the transmission mode and to completely isolate the transmission intermediate frequency during the reception mode.

4. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Na and further in view of Hung et al. (US PAT. 6,370,361 hereinafter, "Hung").

Consider claim 15, Watanabe and Na, in combination, fails to discloses a mode detector configured to detect said transmitting mode and said receiving mode by making & calculation using a first predetermined time slot used for transmission and a second predetermined time slot used for reception.

However, Hung teaches a mode detector configured to detect said transmitting mode and said receiving mode by making & calculation using a first predetermined time slot used for transmission and a second predetermined time slot used for reception (col. 4 lines 54-61).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Hung into view of Watanabe and Na, in order

to provide a transceiver with a receive/transmit fast switch function which can efficiently prevent interference caused during a signal receive/transmit operation by using different receive/transmit intermediate frequency signals.

Consider claims 16-20, Hung further teaches single digital synthesizer driven phase locked loop, in said oscillating state, is configured to receive at least one of a dc-voltage and a ground voltage (col. 4 lines 23-40).

Allowable Subject Matter

5. Claim 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any response to this action should be mailed to:

Mail Stop_____ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

(571) 273-8300

Hand-delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571)272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571)272-7882882. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Nguyen
Examiner
Art Unit 2618

T.N

NAY MAUNG
SUPERVISORY PATENT EXAMINER